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6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.	i .
(a) ☐ including changes required by the Notice of Draftsperson's Patent Dra	rawing Review (PTO-948) attached
1) 🔲 hereto or 2) 🔲 to Paper No./Mail Date	
(b) ☐ including changes required by the attached Examiner's Amendment / Paper No./Mail Date	/ Comment or in the Office action of
identifying indicia such as the application number (see 37 CFR 1.84(c)) should be each sheet. Replacement sheet(s) should be labeled as such in the header accor	
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOG attached Examiner's comment regarding REQUIREMENT FOR THE DEP	
Attachment(s) 1. □ Notice of References Cited (PTO-892) 5. □	☐ Notice of Informal Patent Application (PTO-152)
<u> </u>	Interview Summary (PTO-413),
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), 7. ☐	Paper No./Mail Date Examiner's Amendment/Comment
Paper No./Mail Date4. ☐ Examiner's Comment Regarding Requirement for Deposit 8. ☑	Examiner's Statement of Reasons for Allowance
	Other

Application/Control Number: 09/903,705

Art Unit: 2113

DETAILED ACTION

Allowable Subject Matter

- 1. Claims 1-49 are allowed.
- 2. The following is an examiner's statement of reasons for allowance: The primary reason for the allowance of claims 1-9 is the inclusion of the limitations at least a plurality of processor nodes each having information of relative locations of said processor nodes on said multi-drop bus network; said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; said failure detecting processor node determining from said information of relative locations the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access.

The primary reason for the allowance of claims 10-19 is the inclusion of the limitations each of a plurality of said processor nodes having information providing relative locations of said processor nodes on said multi-drop bus network; said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; said failure detecting processor node determining from said information of relative locations the processor node having failed access which is closest to said failure detecting processor node, and storing an identification of said closest processor node having failed access.

The primary reason for the allowance of claims 20-29 is the inclusion of the limitations a processor independently testing access to other said processor nodes on

said multi-drop bus network; determining from said information table of relative locations the processor not having failed access which is closest to said failure detecting processor node, and storing an identification of said closest processor node having failed access.

The primary reason for the allowance of claims 30-38 is the inclusion of the limitations computer readable program code which causes said computer processor to test independently of other of said processor nodes access to at least one other of said processor nodes on said multi-drop bus network; to determine from said provided information of relative locations the processor node having failed access which is closest to said failure detecting processor node; and computer readable program code which causes said computer processor to store an identification of said closest processor node having failed access.

The primary reason for the allowance of claims 39-49 is the inclusion of the limitations said processor nodes each independently testing access to other said processor nodes on said multi-drop bus network; said failure detecting processor node determining, from said information of relative locations the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably Application/Control Number: 09/903,705

Art Unit: 2113

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accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-

3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 703-

872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Yolanda Wilson Examiner

Art Unit 2113

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ROBERT BEAUSOLIEL

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SUPERVISORY PATENT EXAMINER
FECKAROLOGY CENTER 2100